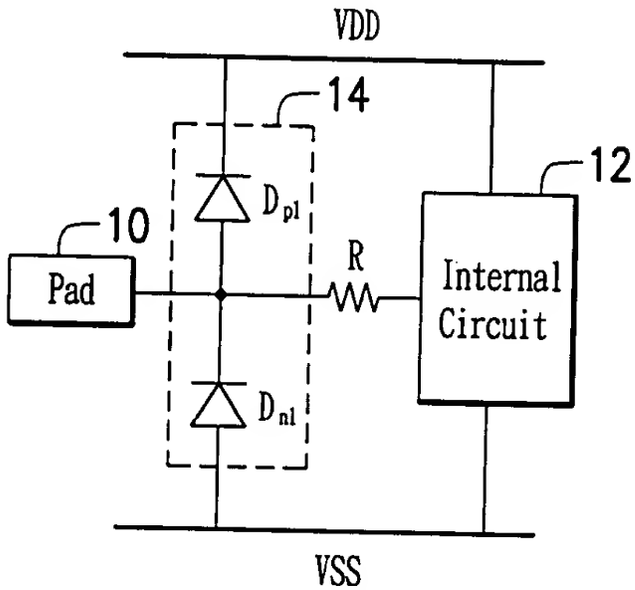


FIG. 1a (PRIOR ART)

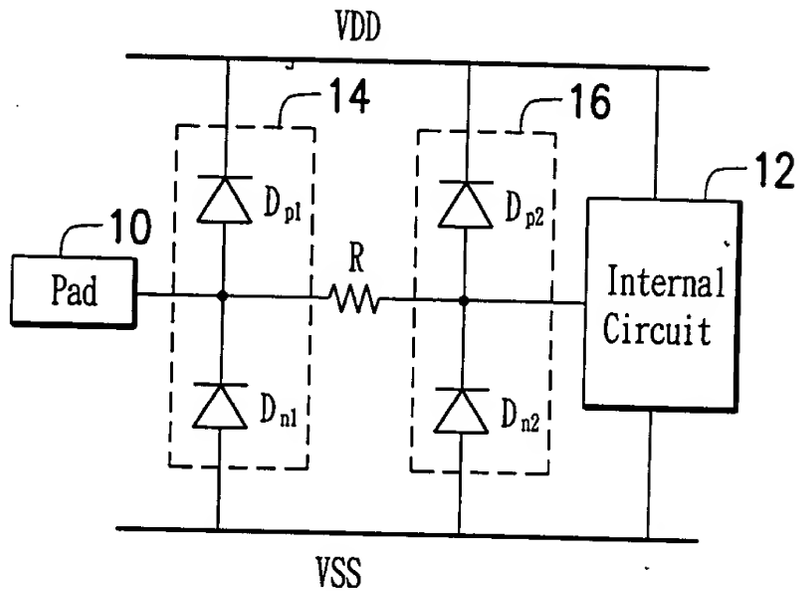


FIG. 1b (PRIOR ART)

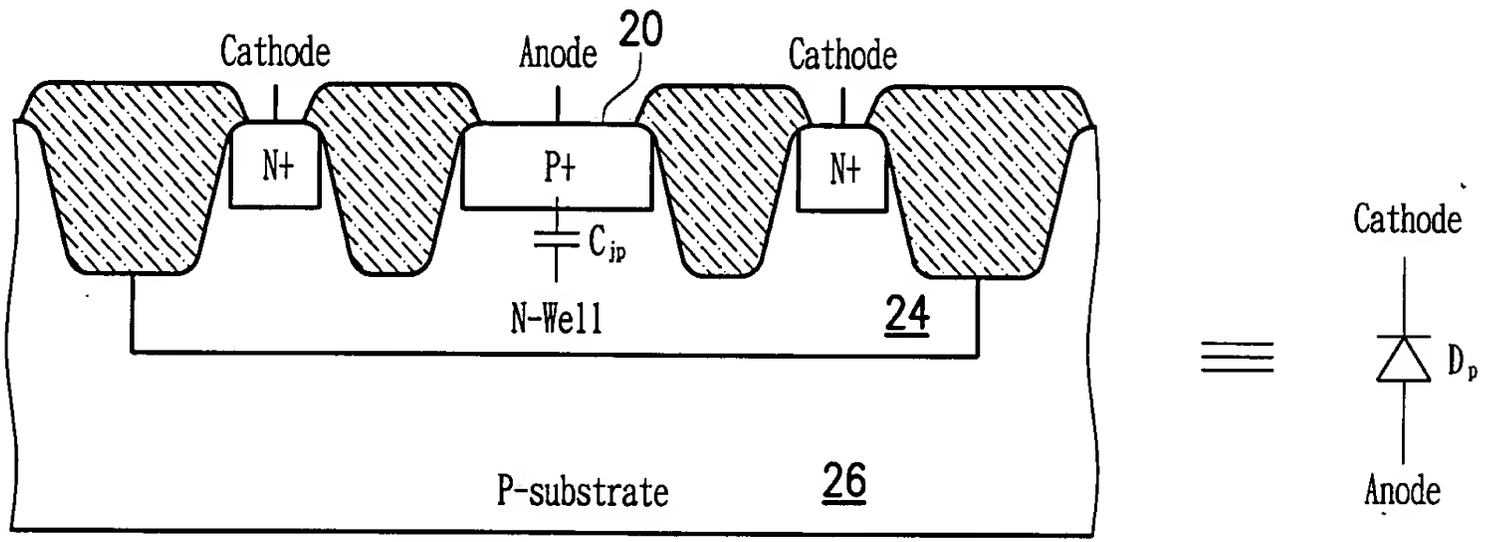


FIG. 2 (PRIOR ART)

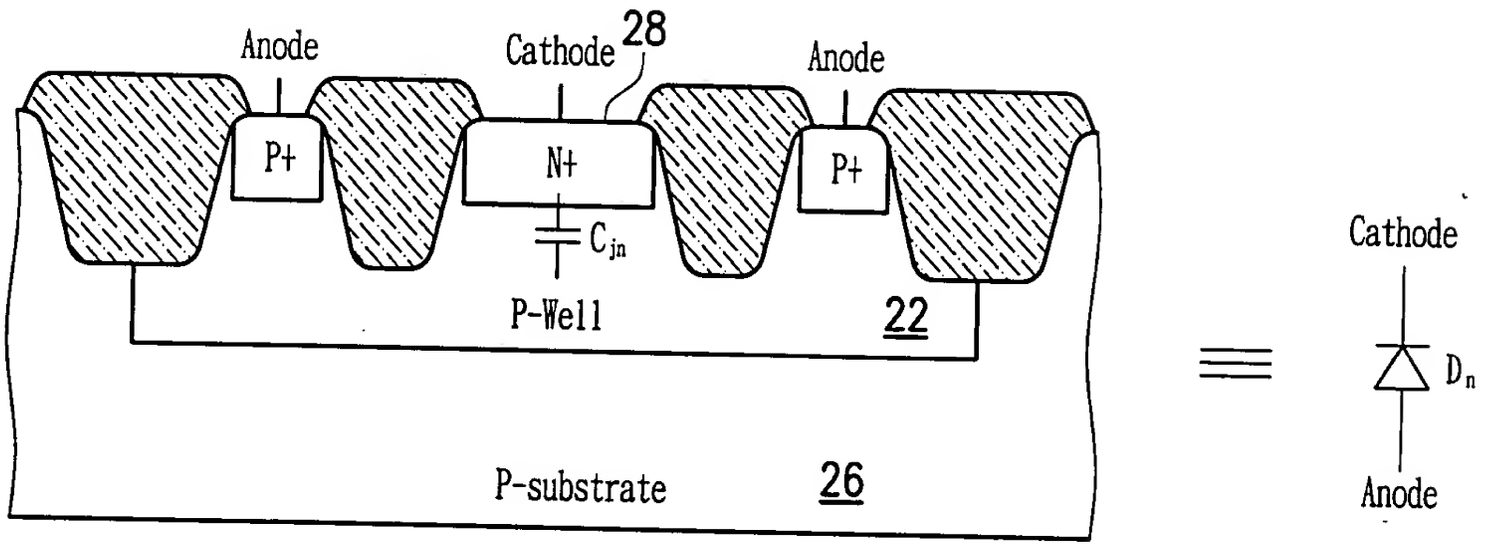


FIG. 3 (PRIOR ART)

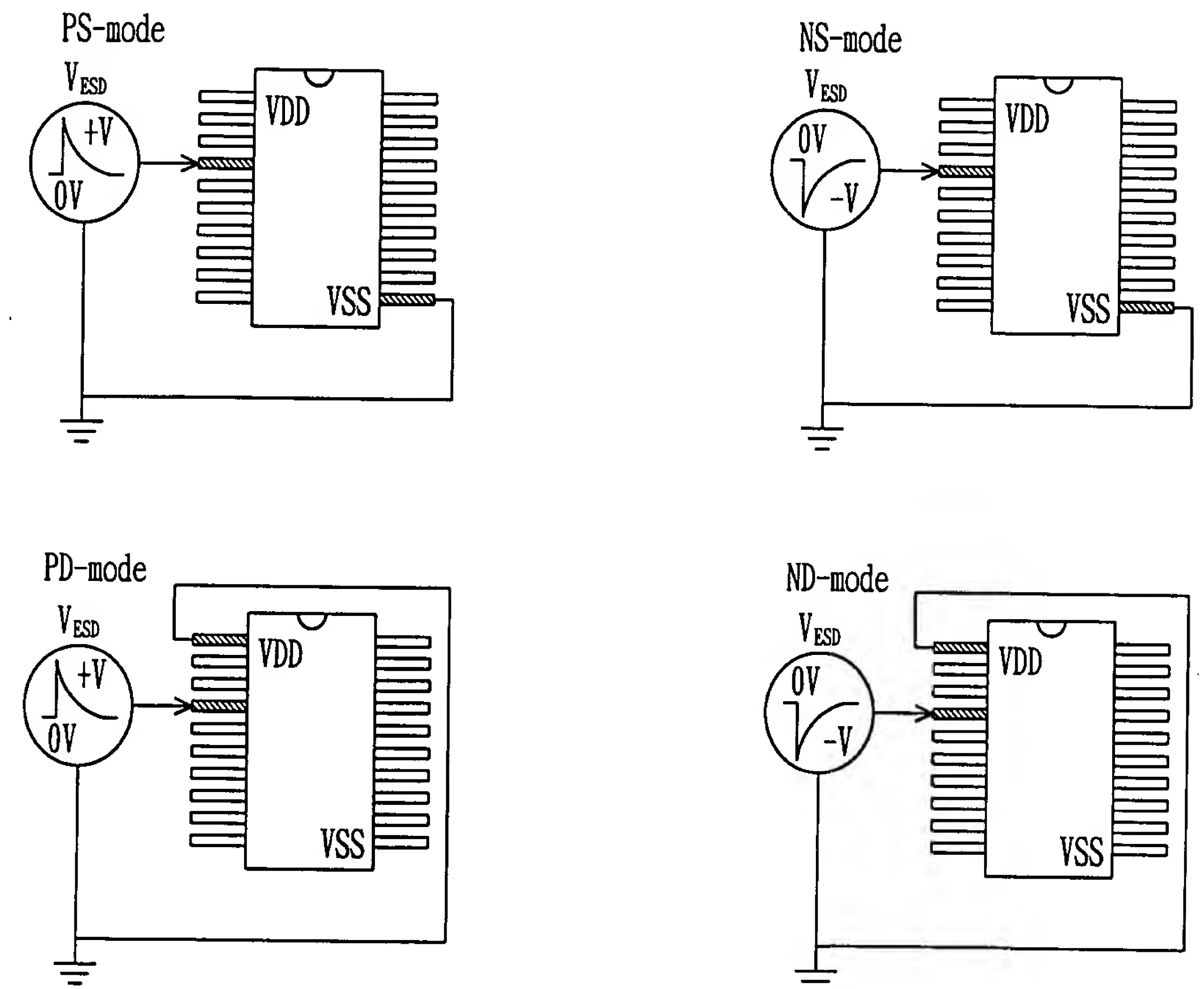


FIG. 4 (PRIOR ART)

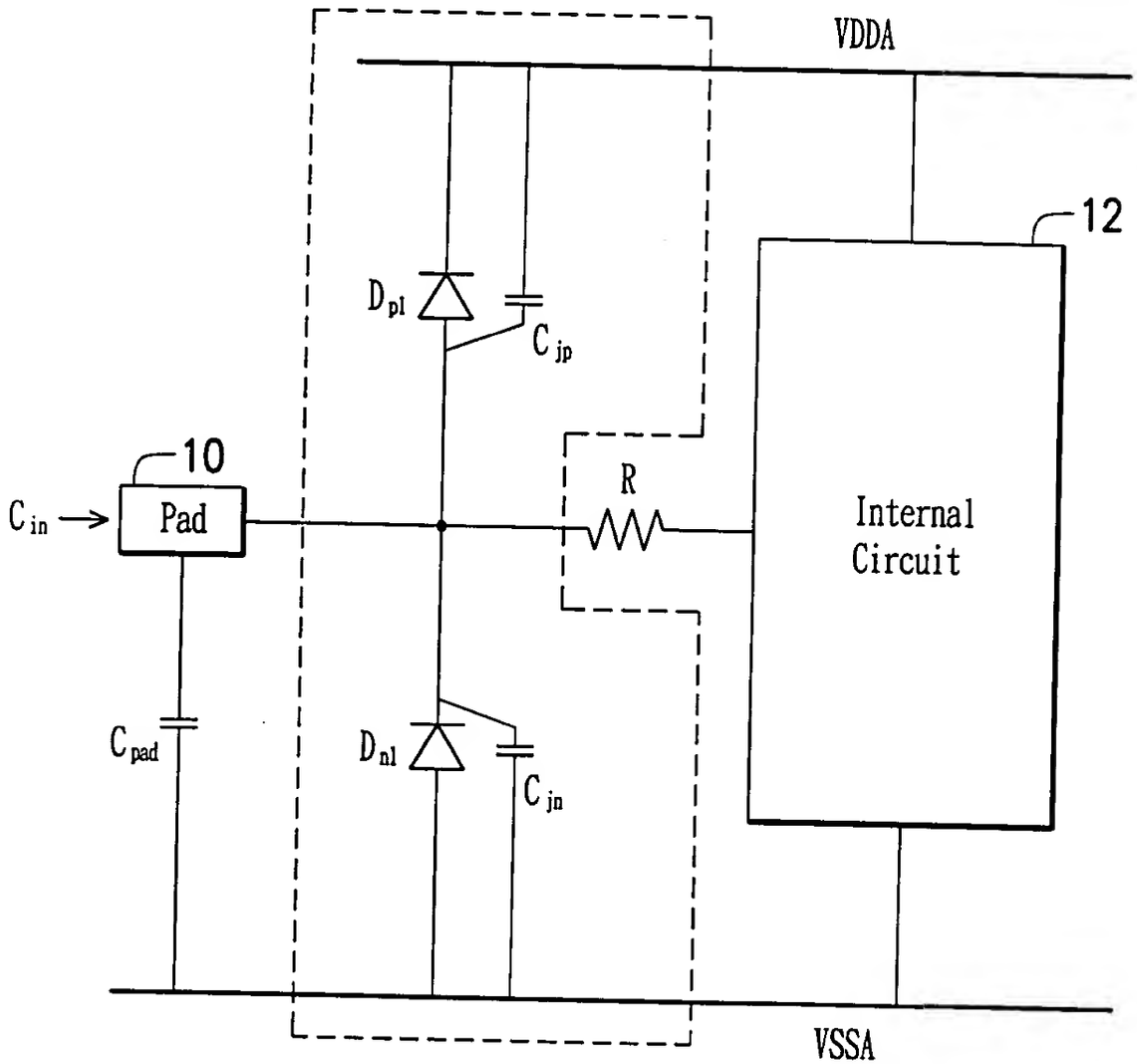


FIG. 5 (PRIOR ART)

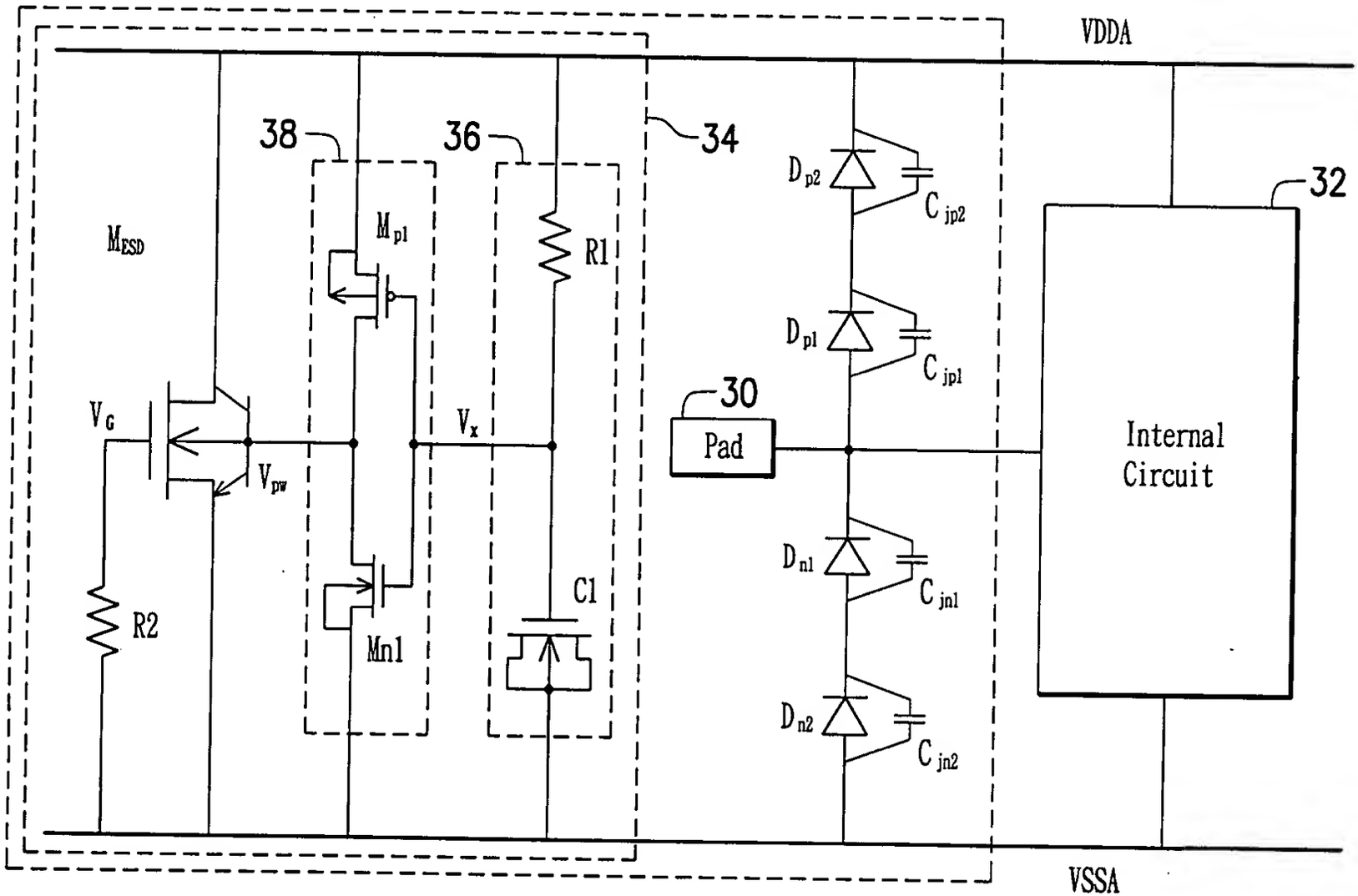


FIG. 6

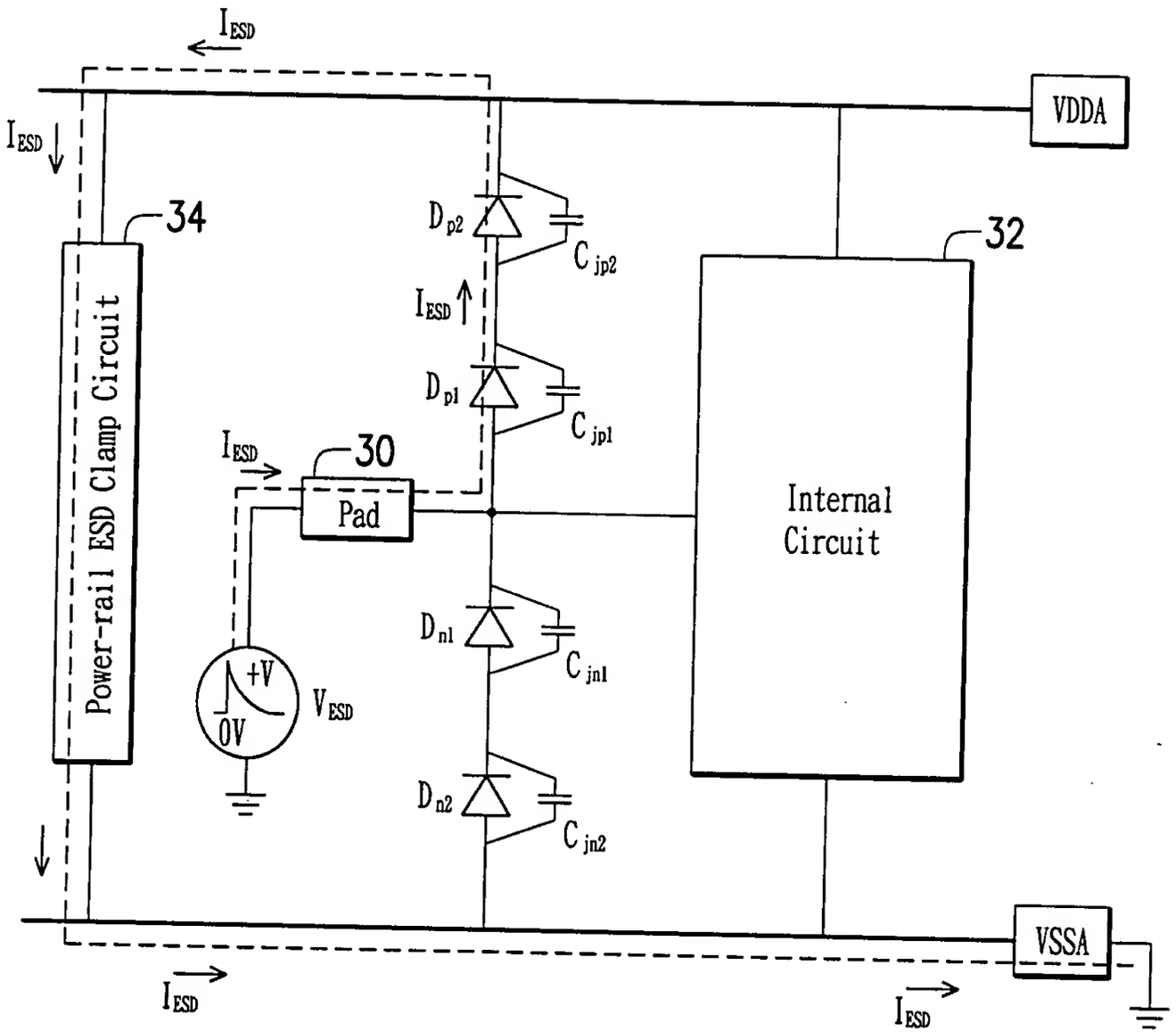


FIG. 7

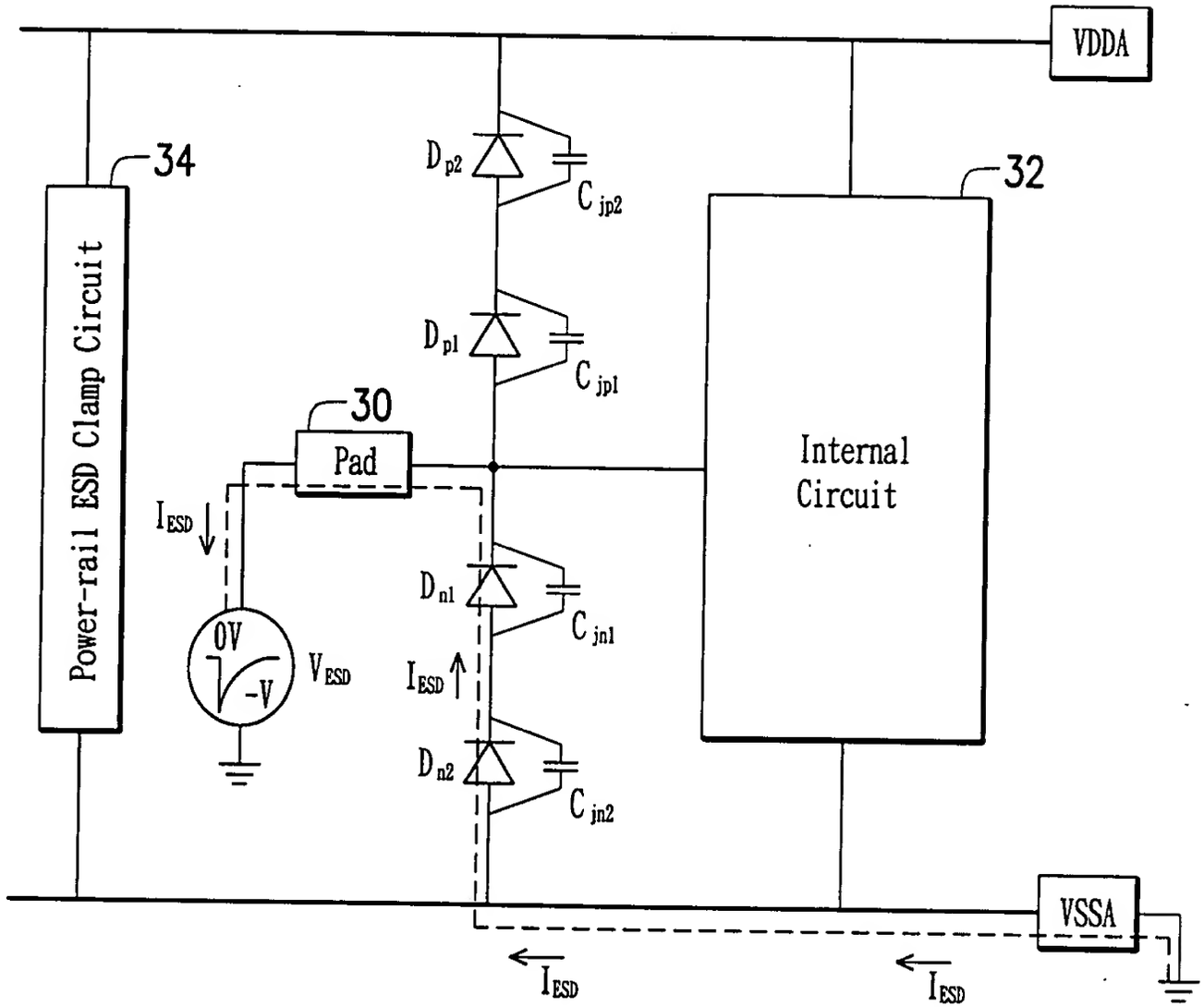


FIG. 8

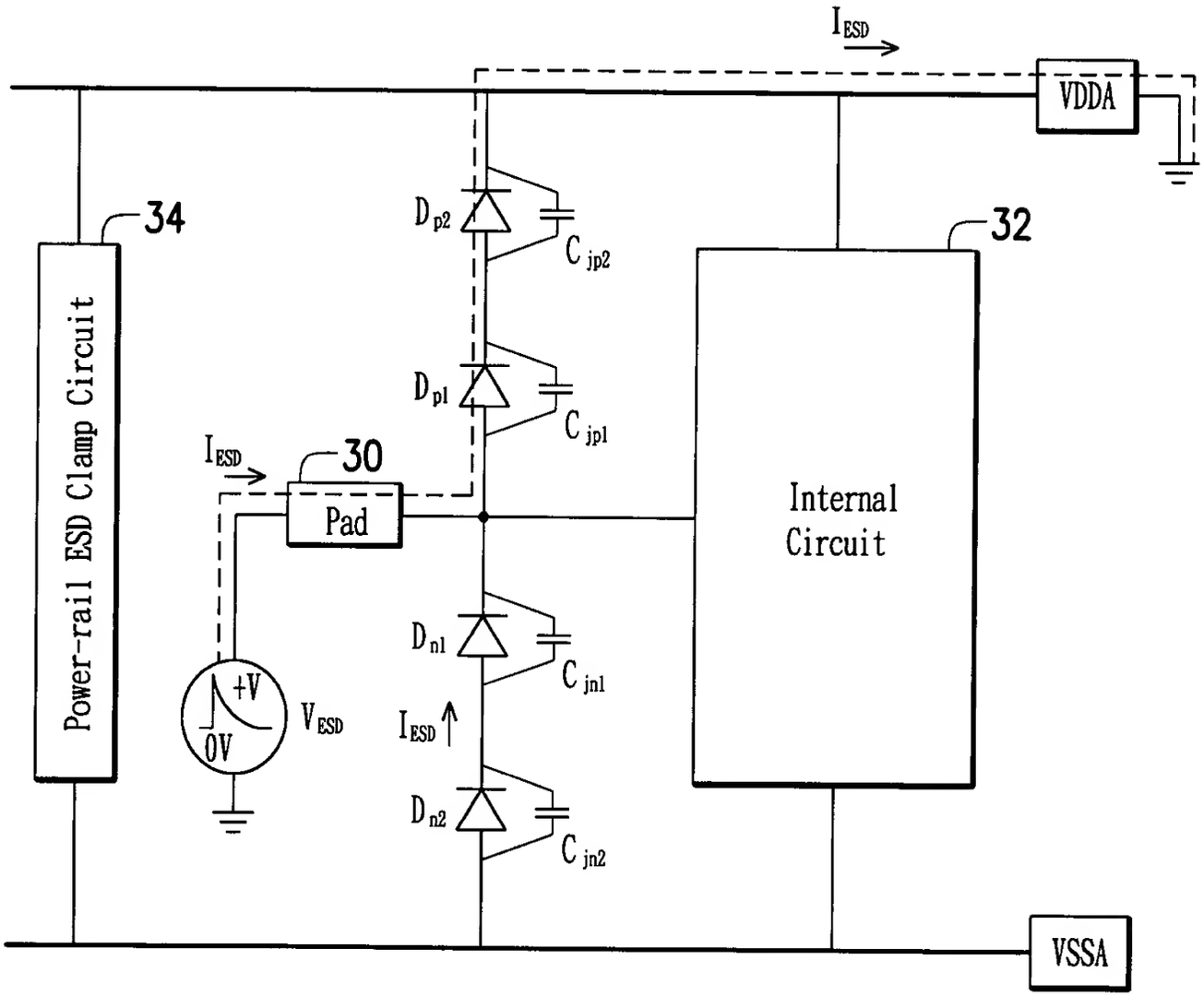


FIG. 9

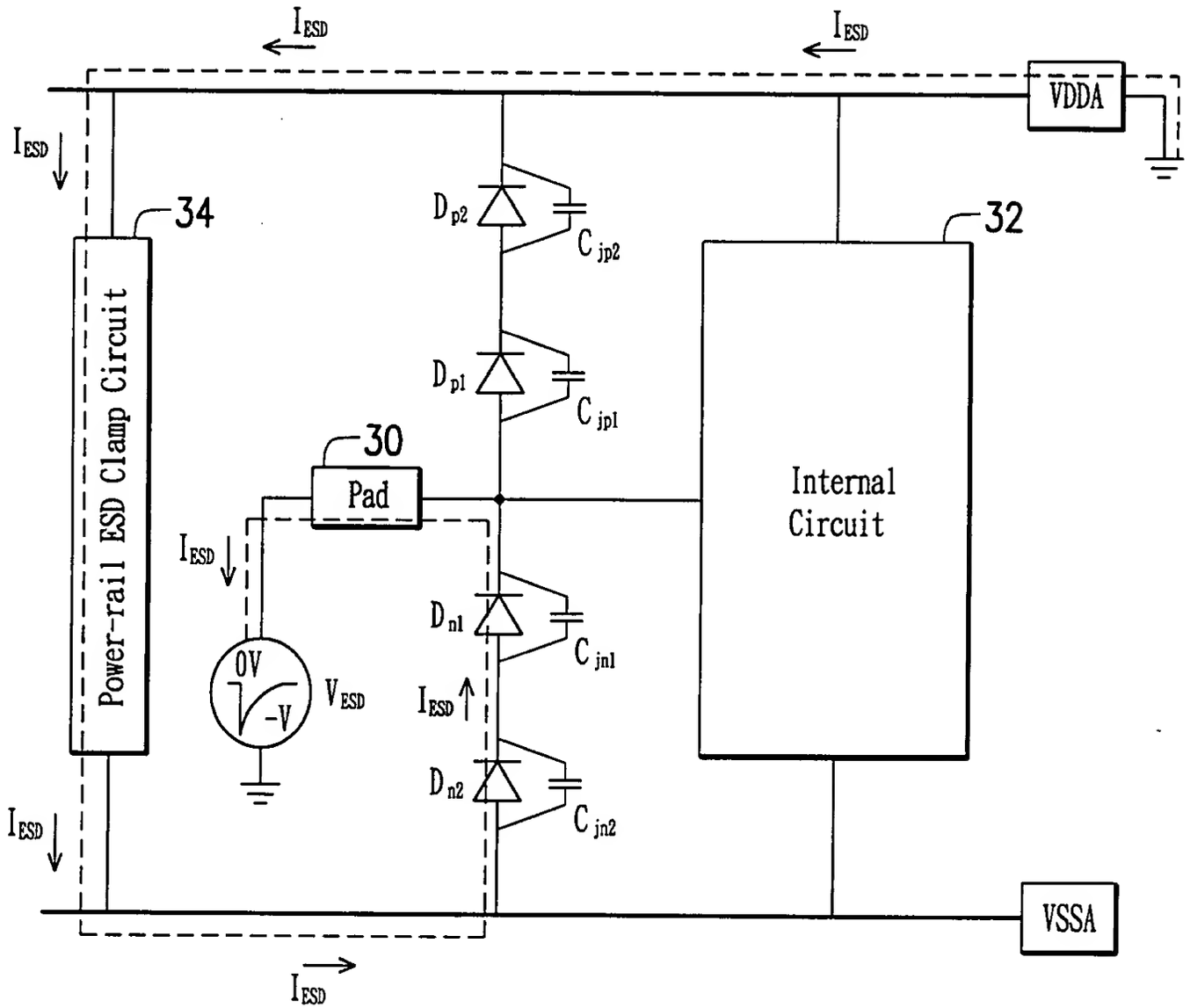

I_{ESD}
I_{ESD}
VDDA
I_{ESD}
34
D_{p2}
C_{jp2}
32
D_{p1}
C_{jp1}
30
Pad
Internal Circuit
Power-rail ESD Clamp Circuit
I_{ESD}
D_{n1}
C_{jn1}
0V
-V
V_{ESD}
I_{ESD}
D_{n2}
C_{jn2}
I_{ESD}
VSSA
I_{ESD}

FIG. 10

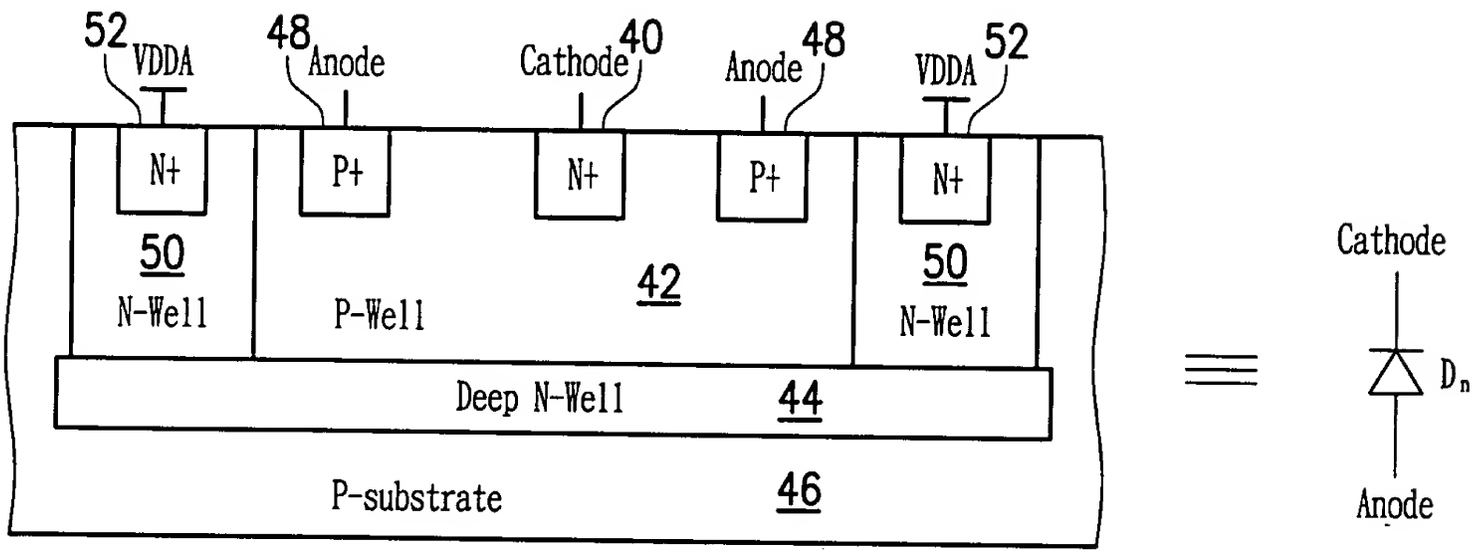


FIG. 11

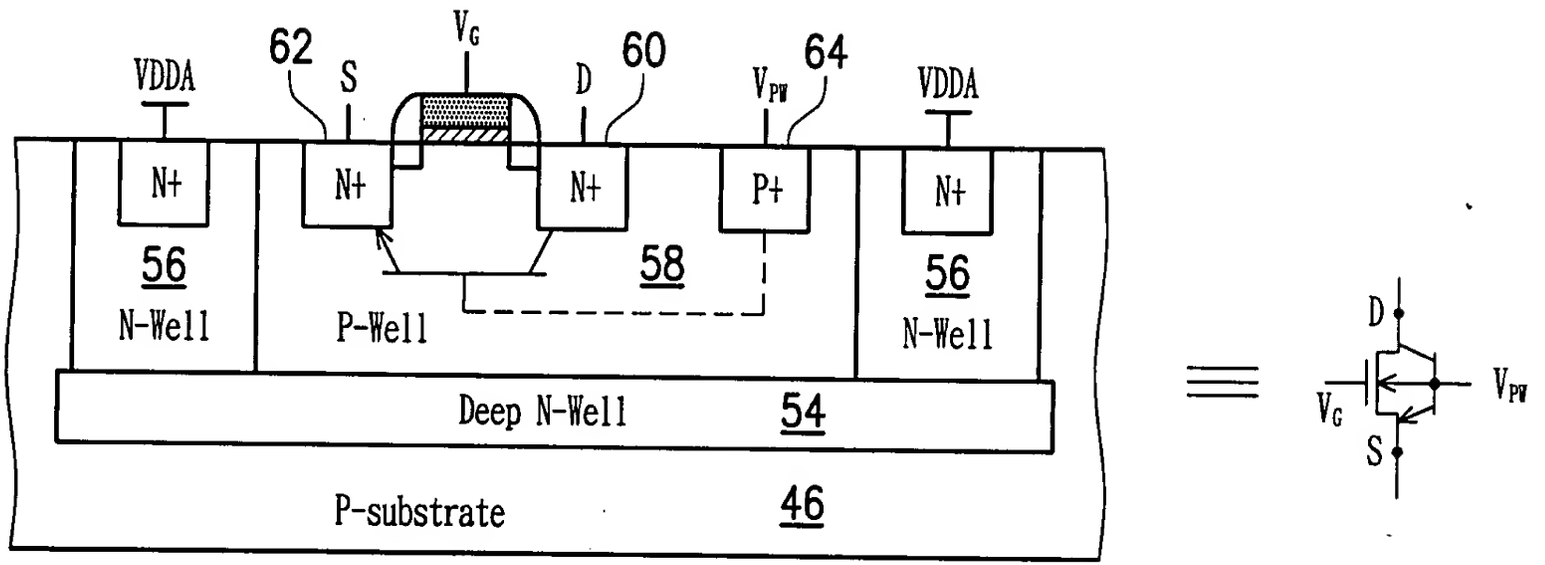


FIG. 12

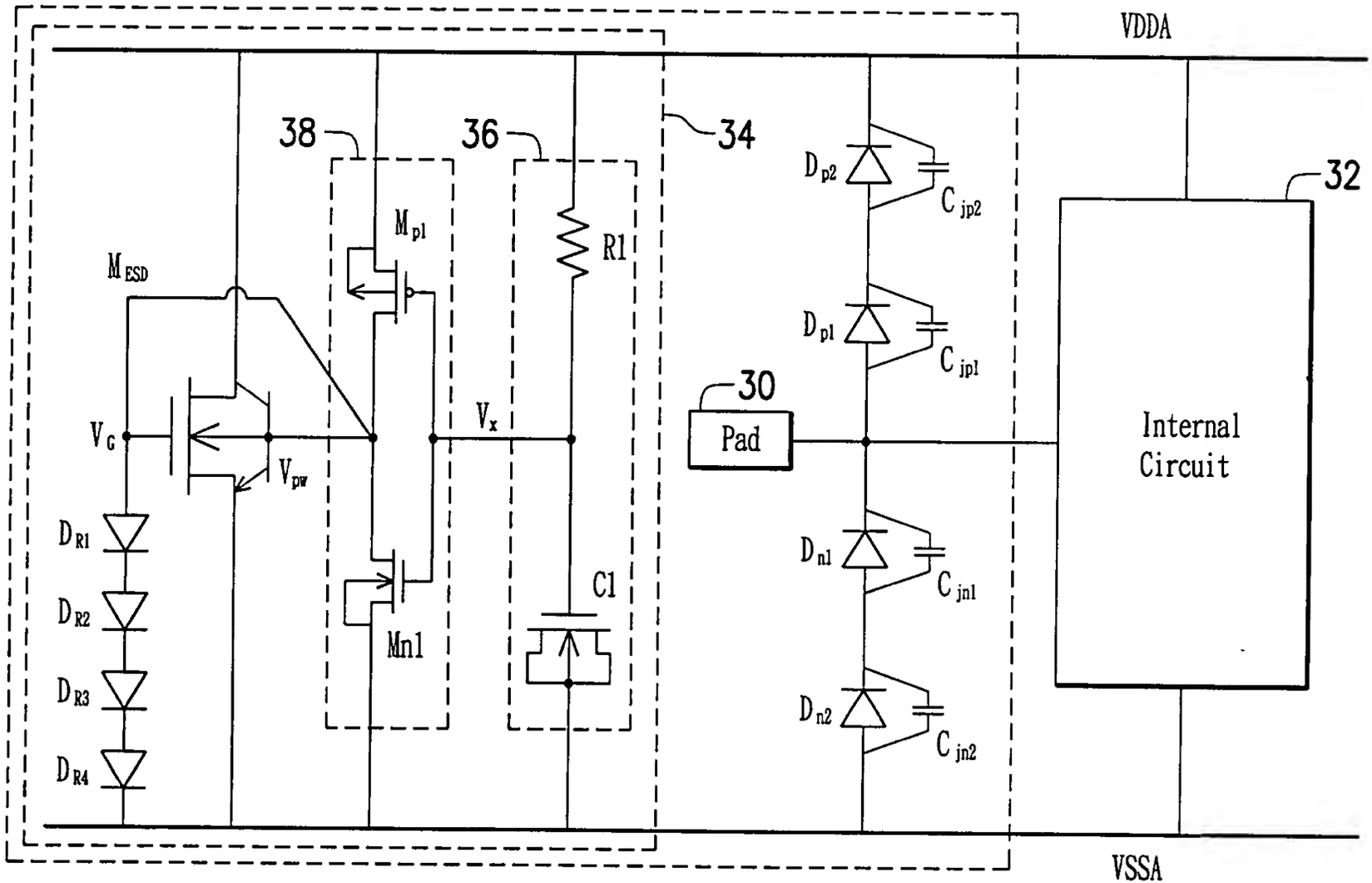


FIG. 13

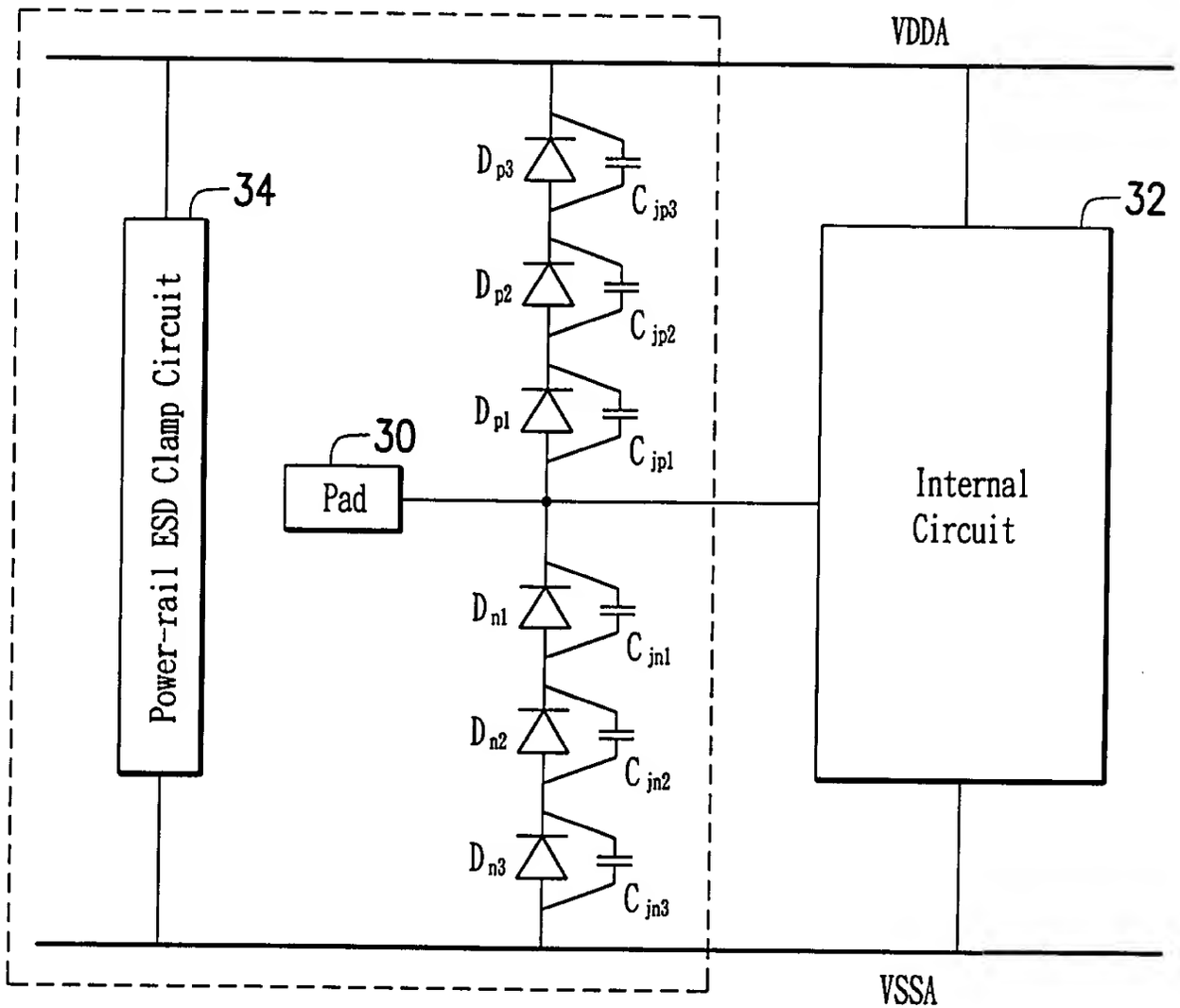


FIG. 14

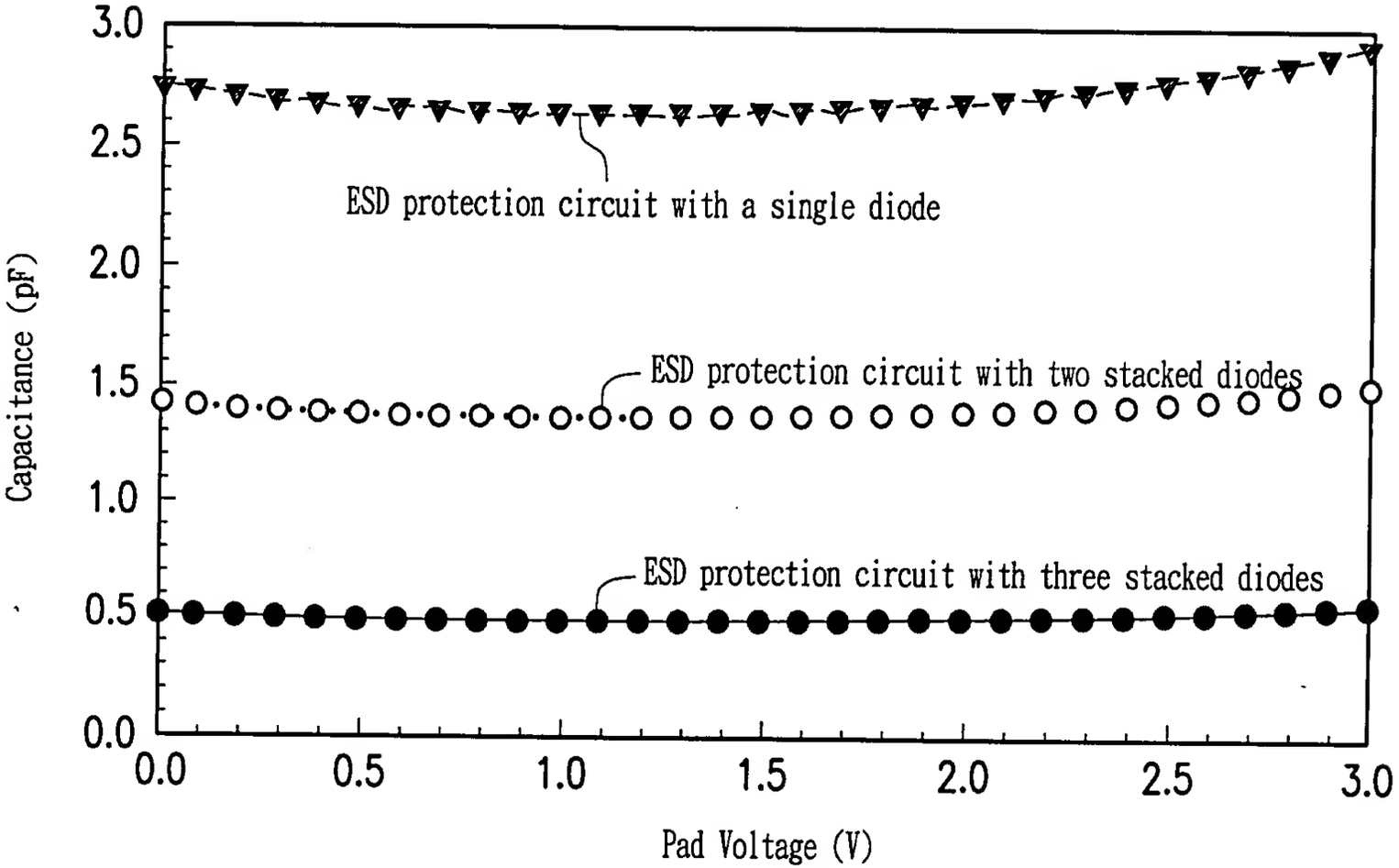

3.0
2.5
2.0
1.5
1.0
0.5
0.0
Capacitance (pF)
ESD protection circuit with a single diode
ESD protection circuit with two stacked diodes
ESD protection circuit with three stacked diodes
0.0
0.5
1.0
1.5
2.0
2.5
3.0
Pad Voltage (V)

FIG. 15

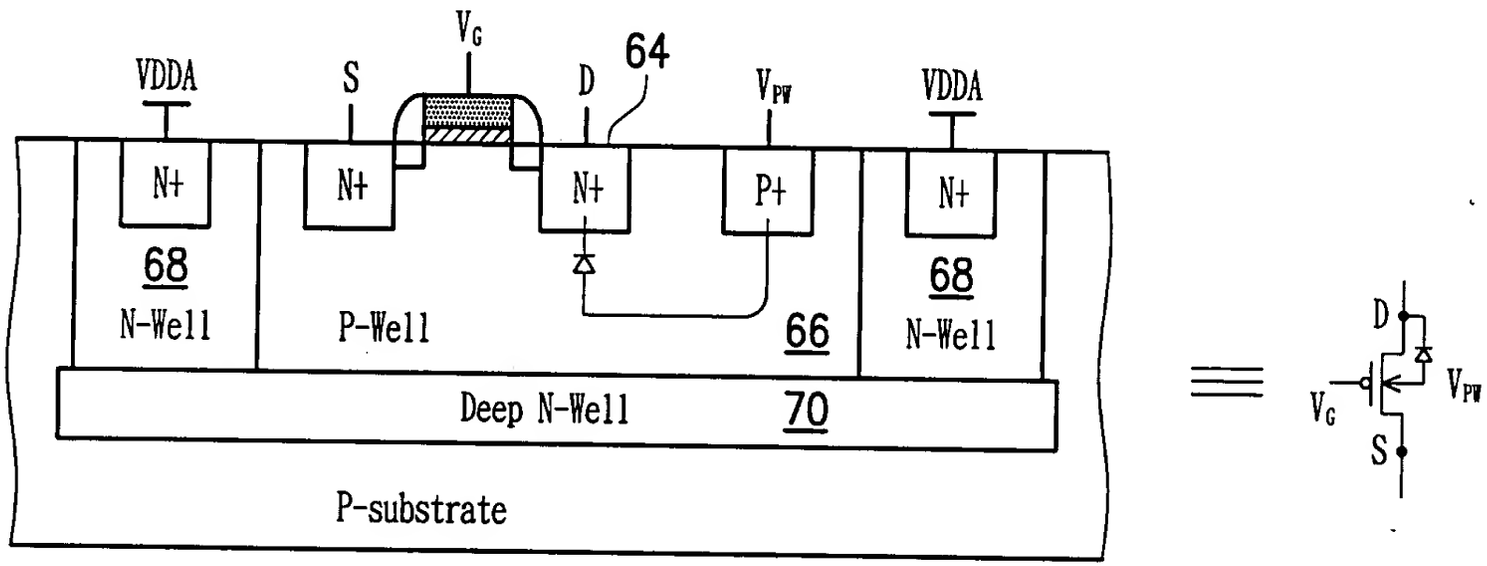


FIG. 16

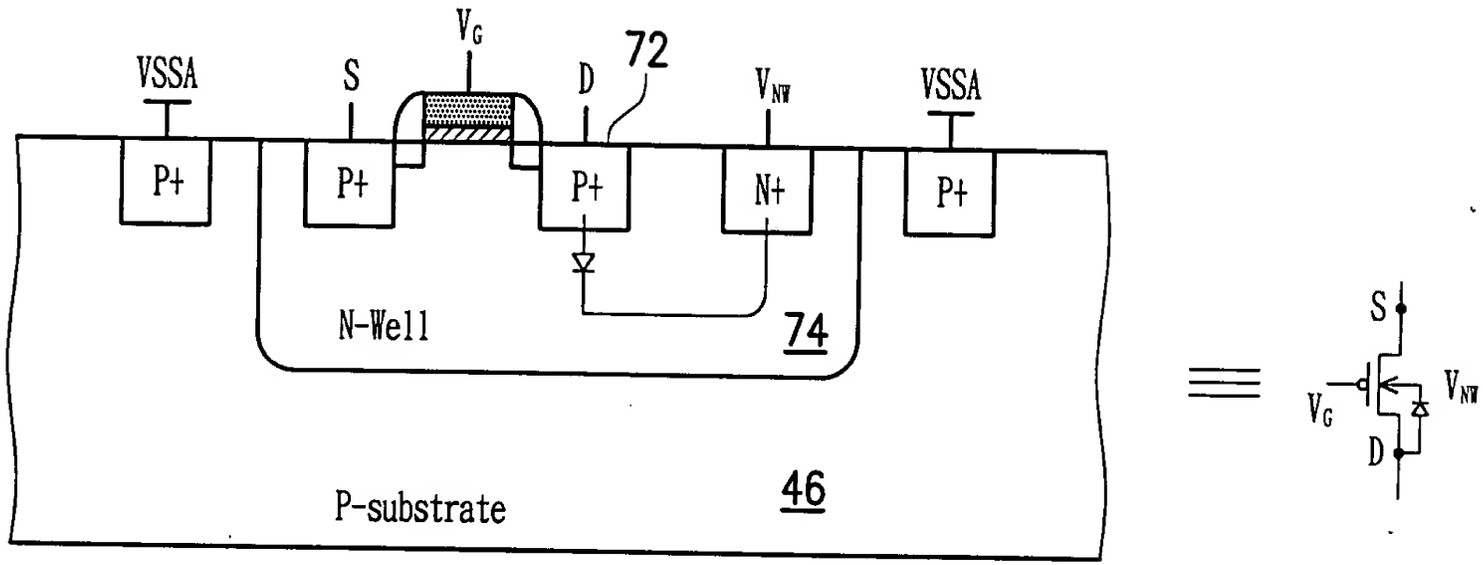


FIG. 17

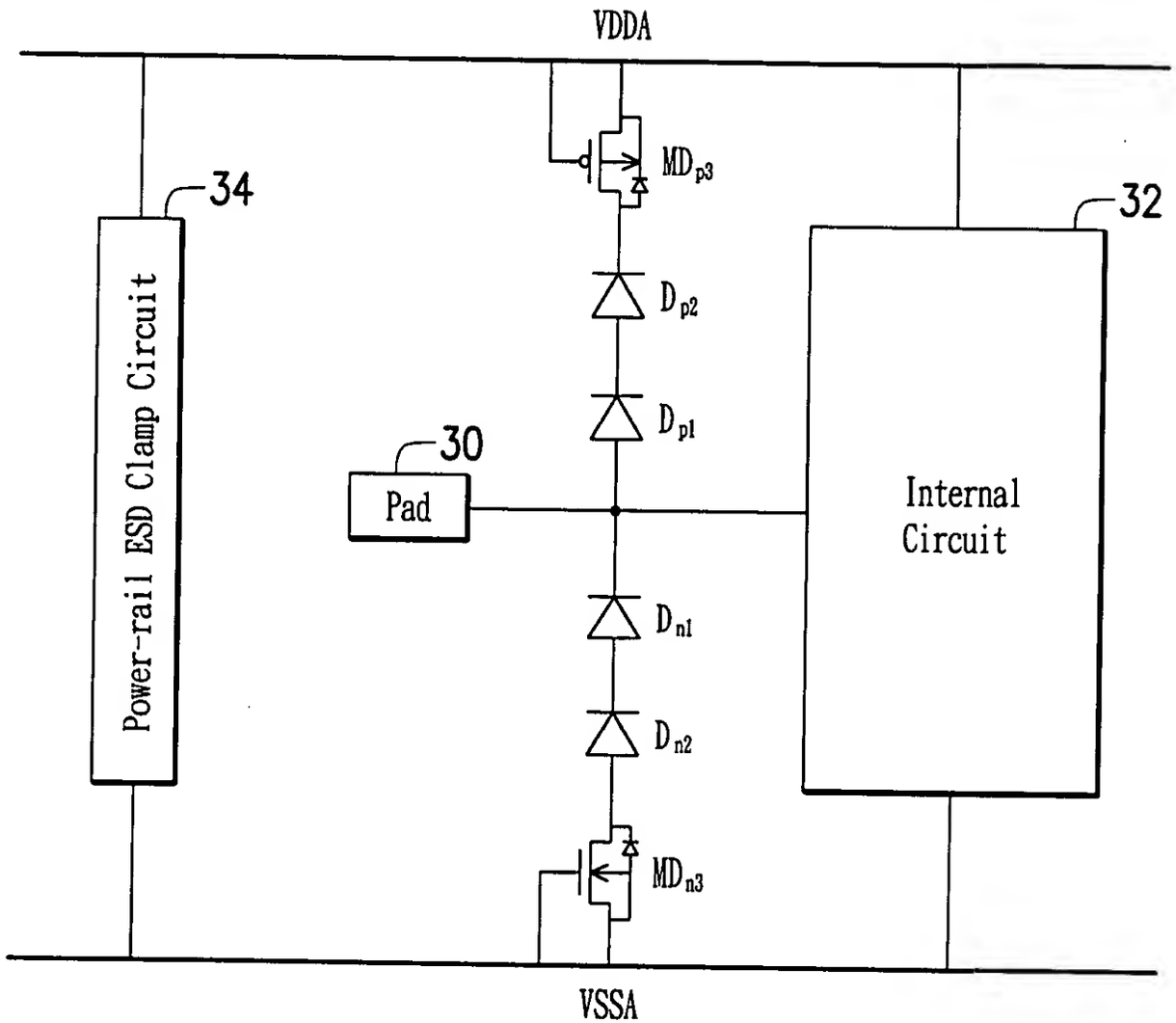

VDDA
34
Power-rail ESD Clamp Circuit
MDp3
Dp2
Dp1
30
Pad
32
Internal Circuit
Dn1
Dn2
MDn3
VSSA

FIG. 18

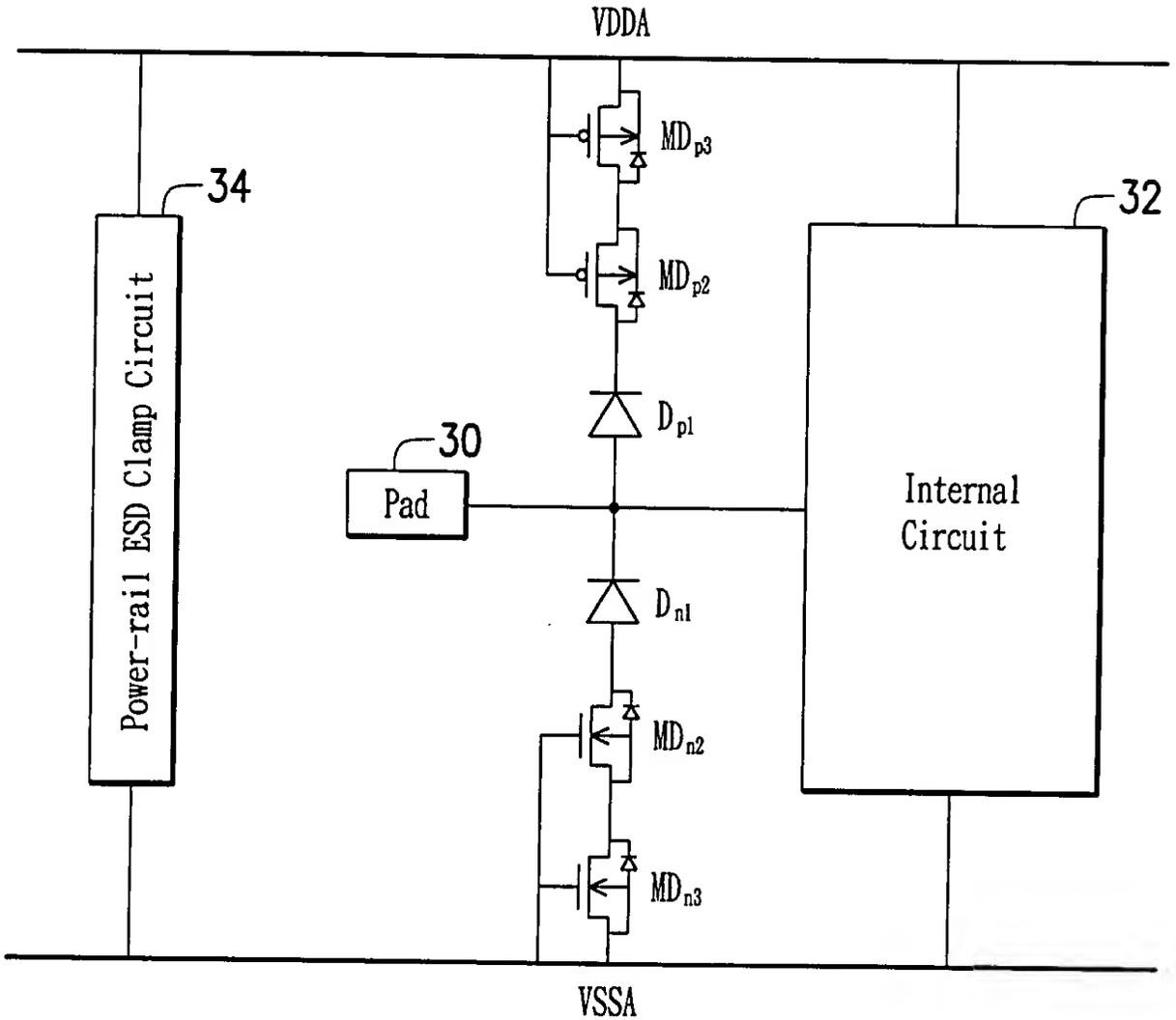


FIG. 19

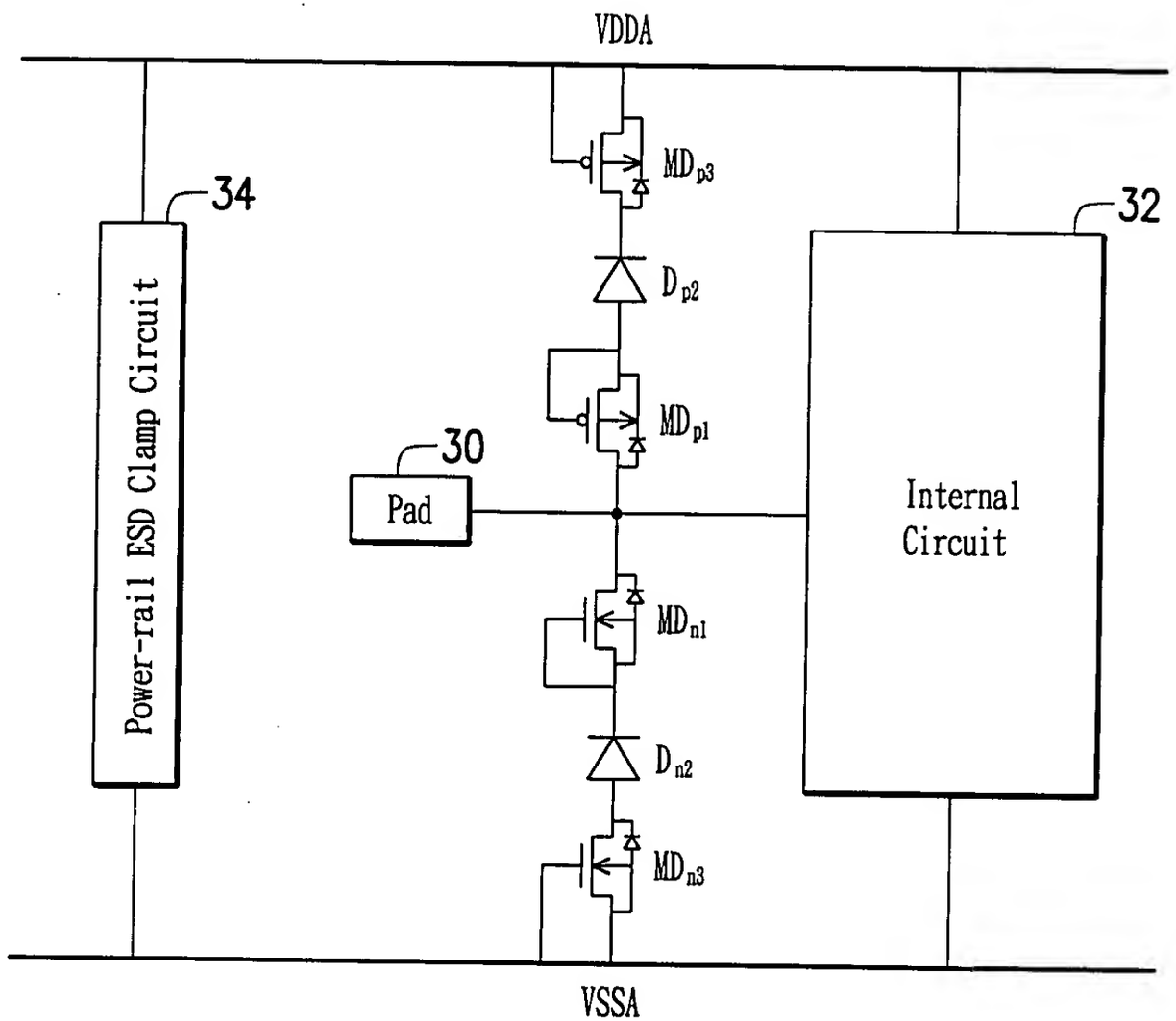


FIG. 20

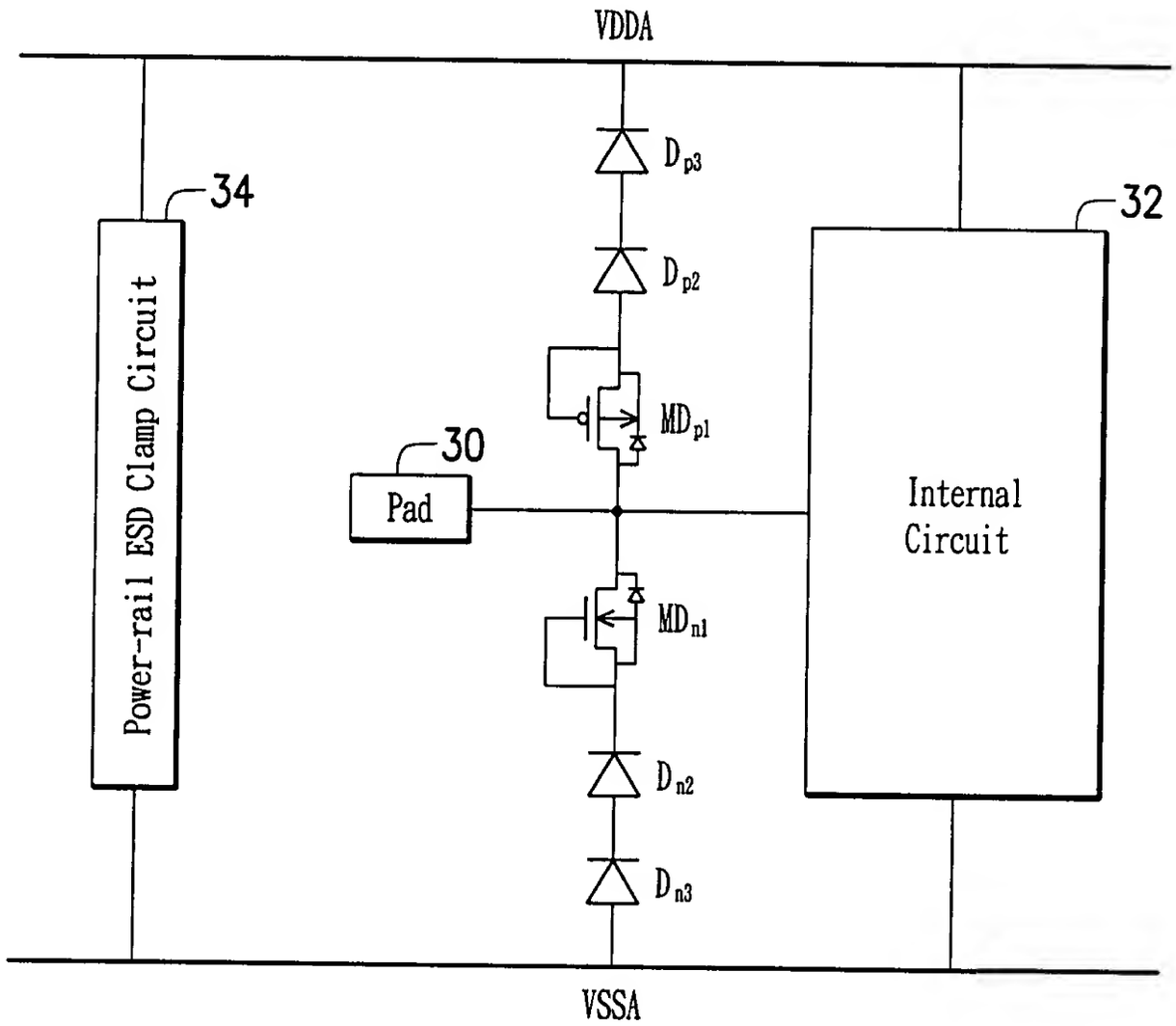
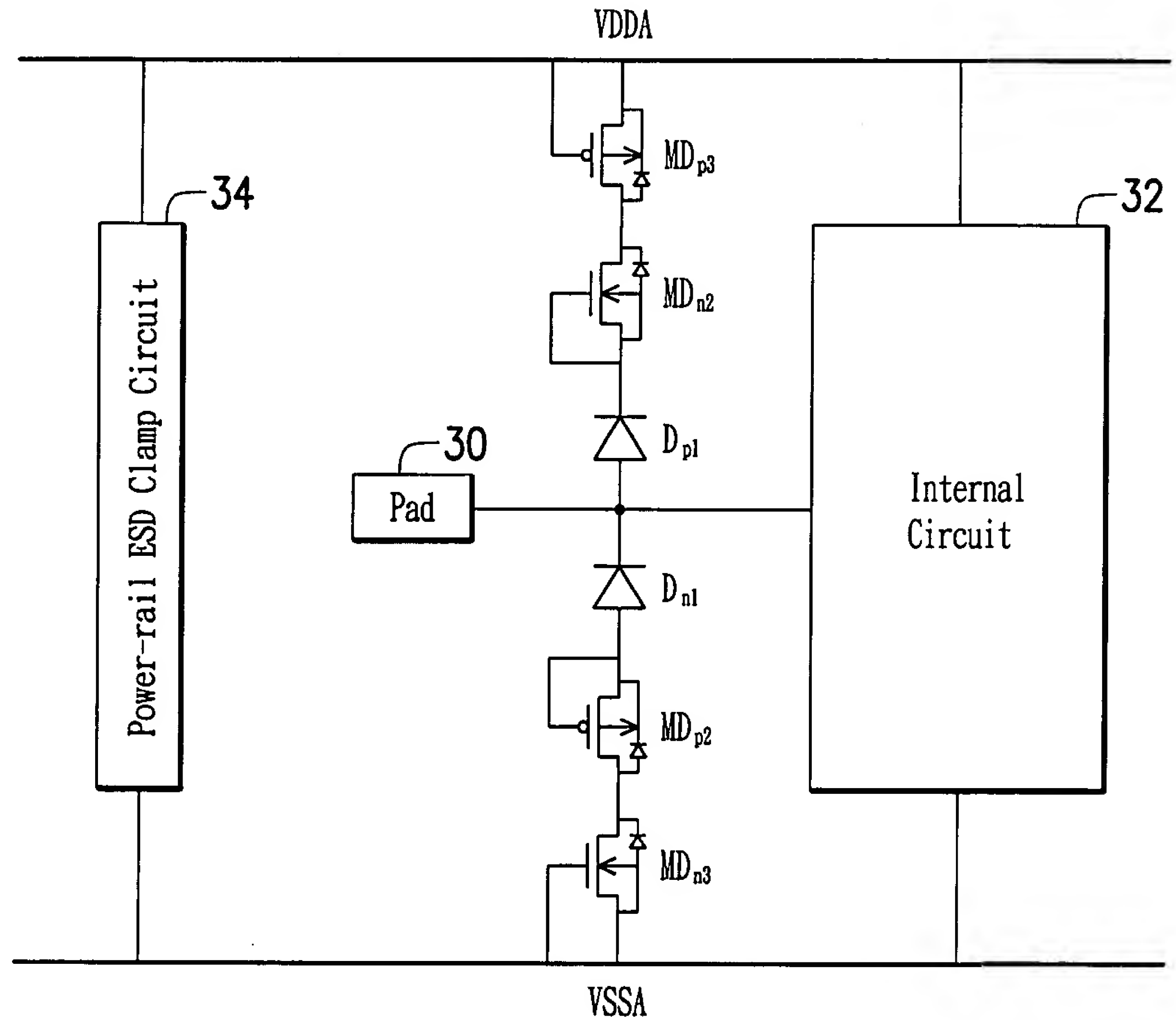


FIG. 21



VDDA
34
Power-rail ESD Clamp Circuit
MDp3
MDn2
Dp1
30
Pad
Dn1
MDp2
MDn3
32
Internal Circuit
VSSA

FIG. 22

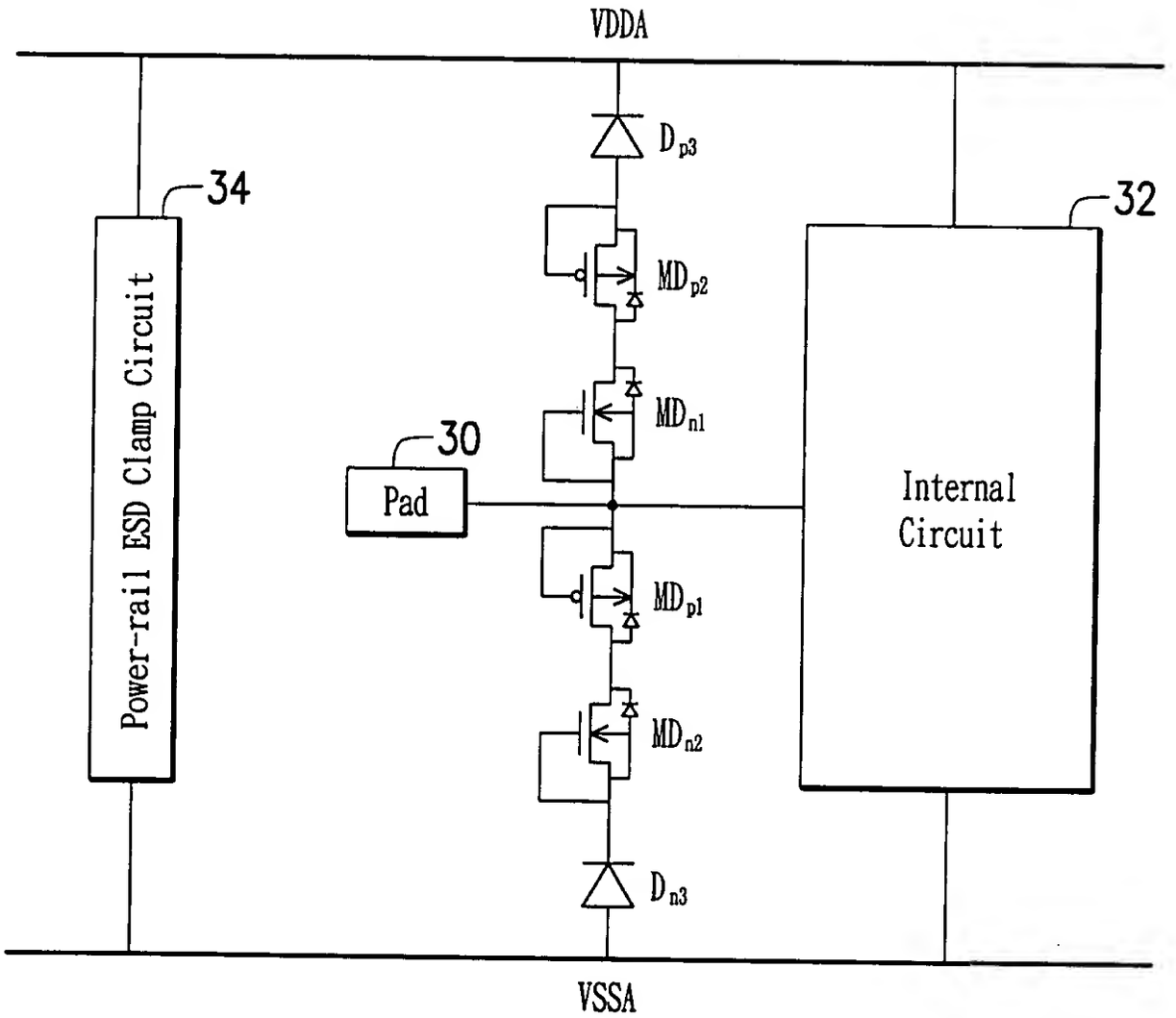


FIG. 23

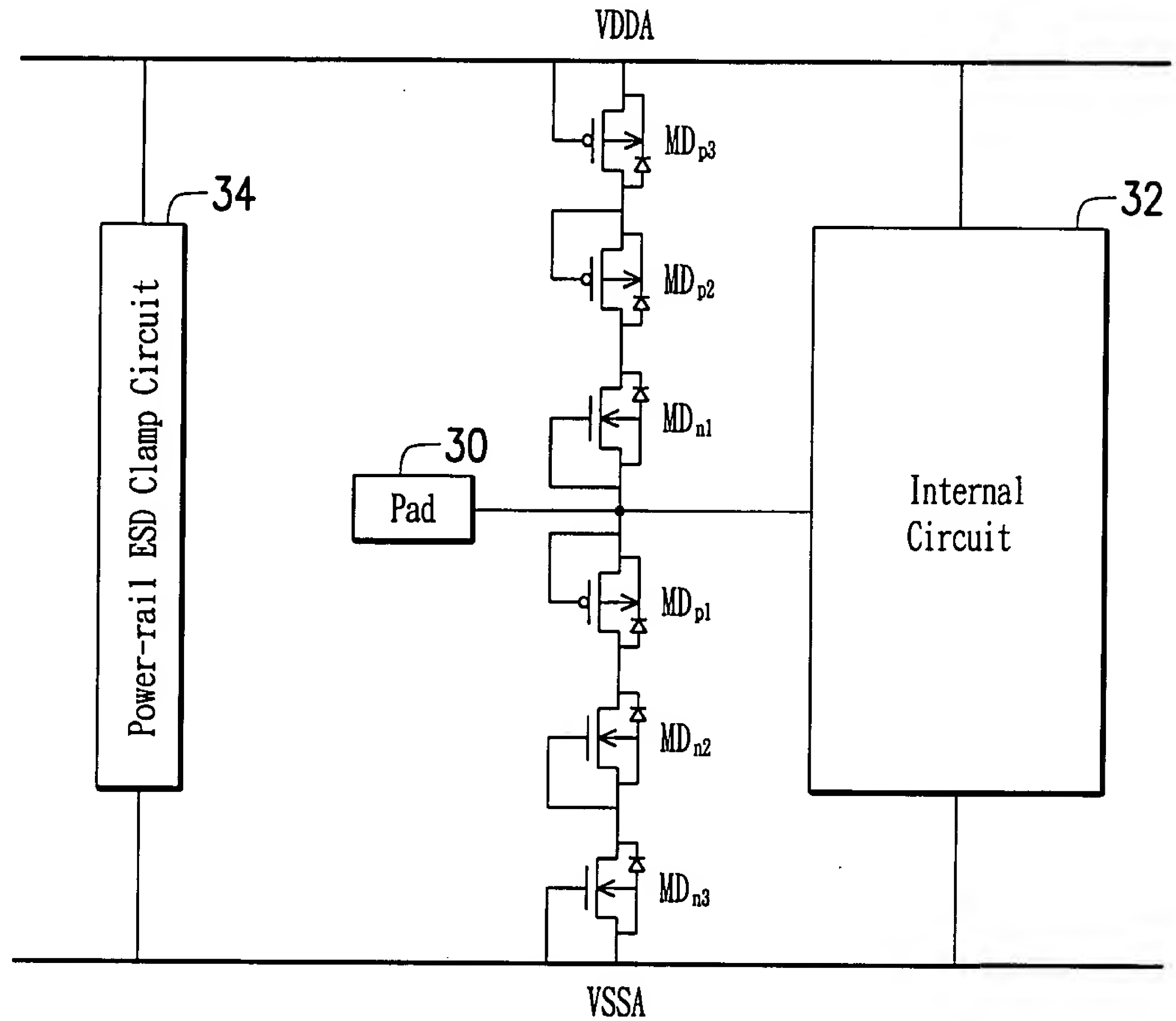

VDDA
MD$_{p3}$
MD$_{p2}$
MD$_{n1}$
MD$_{p1}$
MD$_{n2}$
MD$_{n3}$
VSSA
34
Power-rail ESD Clamp Circuit
30
Pad
32
Internal Circuit

FIG. 24

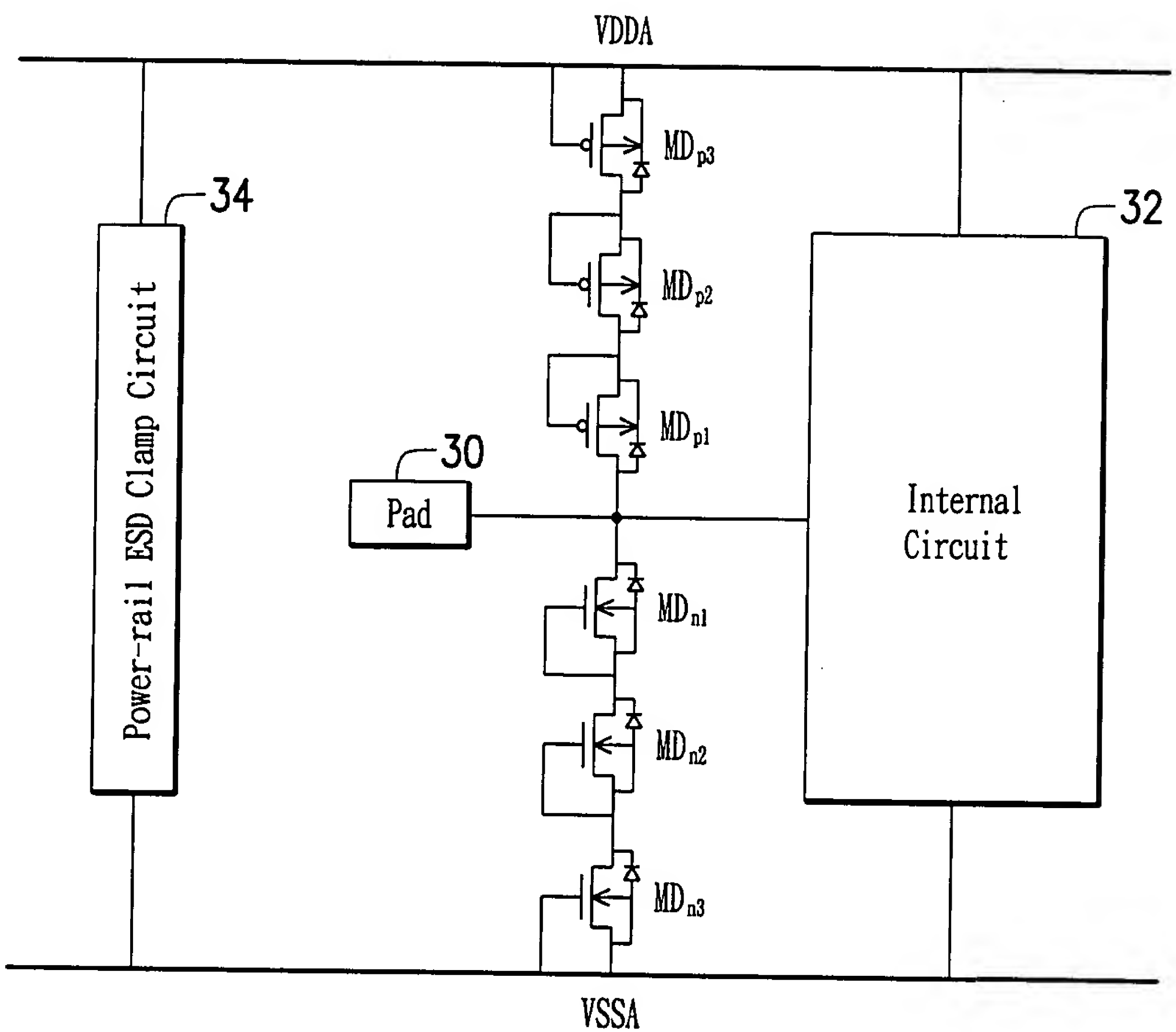

VDDA
34
Power-rail ESD Clamp Circuit
MD_{p3}
MD_{p2}
MD_{p1}
30
Pad
MD_{n1}
MD_{n2}
MD_{n3}
32
Internal
Circuit
VSSA

FIG. 25